REMARKS

This amendment responds to the office action mailed June 14, 2006. In the office action the Examiner:

- allowed claims 1-7;
- objected to claims 21 and 22 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including any limitations of the base claim and any intervening claims;
- rejected claims 8-20 and 23-38 under 35 U.S.C. 102(e) as being anticipated by Stewart et al. (US 2003/0210917 A1) (hereinafter "*Stewart*"); and
- rejected claims 8-14, 17-19, 24-27 and 29 under 35 U.S.C. 102(e) as being anticipated by Chieng et al. (US 6,862,302 B2) (hereinafter "*Chieng*").

After entry of this amendment, the pending claims are: claims 1-19, and 21-38. Applicants have canceled claim 20, amended claims 21, and 23 and have retained the allowed claims in their current form. Applicants believe that the pending claims are now in a condition for allowance.

Claim Objections

The Examiner has objected to claims 21 and 22 as being dependent upon a rejected base claim, but noted that these claims would be allowable if rewritten in independent form including any limitations of the base claim and any intervening claims. Applicants have amended claim 21, which depends from claim 20 to include the limitations of claim 20 and the base claim 14. In light of the above, Applicants believe that claim 21 and its dependant claims are now in a condition for allowance.

Claim Rejections – 35 U.S.C. § 102(e)

The Examiner has rejected claims 8-20 and 23-38 under 35 U.S.C. § 102(e) as being anticipated by *Stewart* and rejected claims 8-14, 17-19, 24-27 and 29 under 35 U.S.C. 102(e) as being anticipated by *Chieng*. In light of the amendments described above, Applicants believe that claims 21, 22, and 23 are now in a condition for allowance and therefore will analyze claim 8-19 and 24-38 in view of Examiner's rejections.

As will be shown below, neither *Stewart* nor *Chieng* are proper prior art references under 35 U.S.C. § 102(e). 35 U.S.C. § 102(e), recites, in pertinent part:

> the invention was described in...an application for patent, published under section 122(b), by *another filed in the United States before the invention* by the applicant for patent or (2) a patent granted on an application for patent by another *filed in the United States before the invention by the applicant* for patent...

The earliest filing date of *Stewart* is April 25, 2002, as this is the filing date of the provisional application to which *Stewart* claims benefit. Similarly, the earliest filing date of *Chieng* is February 12, 2002 as this is the filing date of the provisional application to which *Chieng* claims benefit. However, the present application's earliest filing date is February 5, 2001, based on the parent application (U.S. App. No. 09/777,917, now U.S. Patent No. 7,079,775). Although the present application is a continuation of a continuation-in-part of the patent application, the subject matter of the claims at issue was clearly disclosed in the parent application. As such, the proper priority date to these claims is February 5, 2001, which is earlier than both *Stewart* and *Chieng*. Support for the rejected pending claims can be found in the parent application as follows:

Claim	Examples of support from U.S. 7,079,775
8. An integrated circuit for controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:	Fig. 3
memory, including one or more memory arrays for storing information related to the transceiver in predefined memory mapped locations of the memory, the stored information including digital values corresponding to current operating conditions of the optoelectronic transceiver, where said digital values include a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;	col. 5, lines 4-9.; col. 6, lines 62-66; See also Table 1 See also Fig. 3
analog to digital conversion circuitry for receiving at least one analog signal, the at least one analog signal corresponding to operating conditions of the optoelectronic transceiver, converting the at least one analog signal into at least one digital value, and storing the at least one digital value in at least one of said predefined memory mapped locations in the memory;	col. 4, lines 3-8; col. 6, lines 54-56; col. 7, lines 8-16 See also Fig. 3
control circuitry configured to generate control signals to control operation of the laser transmitter in accordance with one or more values stored in the memory;	col. 3, lines 38-41; col. 5, lines 18-33

an interface for allowing a host to read from host specified locations within the memory, including said predefined memory mapped locations of the memory, so as to obtain one or more of said digital values corresponding to current operating conditions of the optoelectronic transceiver; and	col. 4, line 49 – col. 5, line 3; See also Fig. 3
wherein the control circuitry includes circuitry configured to adjust one or more control signals in accordance with an adjustment value stored in the memory by the host via said interface.	col. 4, lines 15-18; col. 5, lines 18-23
9. The integrated circuit of claim 8, wherein the adjustment value corresponds to a deviation from a configured operating condition of the optoelectronic transceiver	col. 4, lines 15-18; col. 5, lines 18-23
10. The integrated circuit of claim 8, wherein the control circuitry is configured to adjust the one or more control signals by scaling the control signals.	col. 4, lines 15-18; col. 5, lines 18-23
11. The integrated circuit of claim 8, wherein the control circuitry is configured to adjust the one or more control signals by an amount specified by the adjustment value.	col. 4, lines 15-18 col. 5, lines 18-23
12. A method of controlling an optoelectronic transceiver having a laser transmitter and a photodiode receiver, comprising:	col. 1, lines 5-8
in accordance with instructions received from a host device, enabling the host device to read from and write to host specified locations within a controller of the optoelectronic transceiver, the host specified locations including a set of predefined memory mapped locations in which are stored digital values corresponding to current operating conditions of the optoelectronic transceiver, said stored digital values including a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver;	col. 4, line 49 – col. 5, line 9; col. 6, lines 62-66. See also Table 1 See also Fig. 3
receiving a plurality of analog signals from the laser transmitter and photodiode receiver, converting the received analog signals into digital values, and storing the digital values in the controller, the converted digital values including said digital values corresponding to current operating conditions of the optoelectronic transceiver; and	col. 4, lines 3-8; col. 6, lines 51-56; col. 7, lines 8-16 See also Fig. 3
generating control signals to control operation of the laser transmitter in accordance with one or more values stored in predefined memory mapped locations within the controller; and	col. 3, lines 38-41 col. 5, lines 18-23
testing operation of the device at a known deviation from a configured operating condition of the optoelectronic	col. 4, lines 15-18

transceiver by adjusting one or more control signals in accordance with an adjustment value stored in the controller.	
13. The method of claim 12, wherein the adjusting includes scaling the control signals by the adjustment value.	col. 4, lines 15-18 col. 5, lines 18-23
14. A circuit for an optoelectronic transceiver, which includes a laser transmitter and a photodiode receiver, said circuit comprising:	Fig. 2
analog to digital conversion circuitry configured to convert analog signals corresponding to operating conditions of said optoelectronic transceiver into digital values;	col. 4, lines 3-8 col. 6, lines 51-56; col. 7, lines 8-16
memory configured to store said digital values in predefined memory mapped locations, where said digital values stored in said predefined memory mapped locations include: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver; and	col. 5, lines 4-9.; col. 6, lines 62-66. See also Table 1 See also Fig. 3
an interface configured to enable a host to read from said predefined memory mapped locations in memory.	col. 4, line 49 – col. 5, line 9; See also Fig. 3
15. The circuit of claim 14, wherein each of said predefined memory mapped locations are associated with a unique address in said memory.	See e.g. Table 1
16. The circuit of claim 14, wherein each of said digital values is a 16 bit number.	See examples on Table 2 (Bytes 98, 100, 102)
17. The circuit of claim 14, further comprising a temperature sensor for measuring said temperature of said optoelectronic transceiver.	col. 4, lines 1-3; col. 6, lines 11-12; See also Fig. 3
18. The circuit of claim 14, further comprising a supply voltage sensor for measuring said supply voltage of said optoelectronic transceiver.	col. 3, line 52-54; col. 7, line 8-9
19. The circuit of claim 14, wherein said interface is also configured to enable said host to read from and write to host-specified memory mapped addresses within the memory.	col. 4, lines 49-51; See also Fig. 3
24. The circuit of claim 14, further comprising control circuitry configured to generate control signals to control operation of said laser transmitter in accordance with one or more values stored in memory.	col. 3, lines 38-41; col. 5-, line 18-23
25. The circuit of claim 24, wherein said control circuitry includes operation disable circuitry configured to disable operation of at least part of said optoelectronic transceiver.	col. 8, lines 7-18
26. The circuit of claim 14, wherein said memory further comprises one or more memory arrays for storing information related to said optoelectronic transceiver.	col. 5, lines 4-9.; col. 6, lines 62-66. See also Table 1; Fig. 3

27. The circuit of claim 14, wherein a portion of said memory is reserved for optional warning flags.	Table 1; col. 7, line 30 – col. 8, line 3 Fig. 3
28. The circuit of claim 27, wherein said optional warning flags are selected from a group consisting of: a temperature high warning, a temperature low warning, a high supply voltage warning, a low supply voltage warning, a high laser bias current warning, a low laser bias current warning, a high output power warning, a low output power warning, a high received optical power warning, and a low received optical power warning.	Table 3 col. 8, lines 19-25
29. The circuit of claim 14, wherein a portion of said memory is reserved for optional alarm flags.	col. 7, line 30 – col. 8, line 3 Table 1 (memory locations 70h-73h, 74h-77h) Table 3
30. The circuit of claim 29, wherein said optional alarm flags are selected from a group consisting of: a temperature high alarm, a temperature low alarm, a high supply voltage alarm, a low supply voltage alarm, a high laser bias current alarm, a low laser bias current alarm, a high output power alarm, a low output power alarm, a high received optical power alarm, and a low received optical power alarm.	Table 3 col. 8, lines 19-25
31. The circuit of claim 14, wherein a portion of said memory is reserved for an optional indication of a state of a transmitter disable input pin.	col. 4, lines 45-49; col. 8, lines 7-18; Table 2 (Byte 110, Bit 7)
32. The circuit of claim 14, wherein a portion of said memory is reserved for an optional indication of a state of a software disable.	col. 4, lines 45-49; col. 8, lines 7-18; Table 2 (Byte 110, Bit 7)
33. The circuit of claim 14, wherein a portion of said memory is reserved for a password that controls access to said memory.	Table 1 (memory location 7Bh-7Eh)
34. A circuit for an optoelectronic transceiver, comprising:	Fig. 2
analog to digital conversion circuitry configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into 16 bit digital values;	col. 4, lines 3-8 col. 6, lines 51-56; col. 7, lines 8-16; Fig. 3
memory configured to store said digital values in predefined memory mapped locations identified by unique addresses, where said digital values comprise: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of a laser transmitter of said optoelectronic transceiver, an output power of said laser transmitter, and a received optical power of a photodiode receiver of said optoelectronic transceiver; and	col. 5, lines 4-9.; col. 6, lines 62-66. See also Table 1 See also Fig. 3
an interface configured to enable a host having said addresses to read said digital values from said predefined	col. 4, line 49 – col. 5, line 9; See also Fig. 3

memory mapped locations in memory.	
35. The circuit of claim 34, further comprising: a temperature sensor for measuring said temperature of said optoelectronic transceiver; and a supply voltage sensor for measuring said internal supply voltage of said optoelectronic transceiver.	 col. 4, lines 1-3; col. 6, lines 11-12; See also Fig. 3 col. 3, line 52-54; col. 7, lines 8-9
36. The circuit of claim 34, wherein said interface is also configured to enable said host to read from and write to host-specified memory-mapped locations within the memory.	col. 4, line 49 – col. 5, line 3 See also Fig. 3
37. The circuit of claim 34, wherein a portion of said memory is reserved for information selected from a group consisting of: optional warning flags, optional alarm flags, an optional indication of a state of a transmitter disable input pin, an optional indication of a state of a software disable feature of said optoelectronic transceiver, and a password that controls access to said memory.	Table 1 (memory locations 70h-73h, 74h-77h, 7Bh-7Eh) Table 2 (Byte 110) Table 3
38. An optoelectronic transceiver, comprising: a housing; a laser transmitter at least partially contained within said housing; a photodiode receiver at least partially contained within said housing; circuitry at least partially contained, said circuitry comprising: analog to digital conversion circuitry configured to convert analog signals corresponding to operating conditions of an optoelectronic transceiver into digital values; memory configured to store said digital values in predefined memory mapped locations identified by unique addresses, where said digital values comprise: a temperature of said optoelectronic transceiver, an internal supply voltage of said optoelectronic transceiver, a laser bias current of said laser transmitter, an output power of said laser transmitter, and a received optical power of said photodiode receiver; and an interface configured to enable a host having said addresses to read said digital values from said predefined memory mapped locations in memory	 See Figs. 1 and 2 col. 4, lines 3-8 See also Fig. 3 col. 5, lines 4-9.; col. 6, lines 62-66. See also Table 1 See also Fig. 3 col. 4, lines 49-51; See also Fig. 3

In light of the forgoing, neither *Stewart* and *Chieng* are proper prior art references as they were filed after the earliest filing date of the present application. Therefore, Applicants respectfully request that the Examiner withdraw her rejections with regard to rejected claims 8-19 and 24-38.

Conclusion

In light of the above amendments and remarks, the Applicant respectfully requests that the Examiner reconsider this application with a view towards allowance. The Examiner is invited to call the undersigned attorney at 650-843-4000 if a telephone call could help resolve any remaining items.

Respectfully submitted,

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